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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,183	02/27/2004	Kenji Sakaue	249418US2S	4589

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
GUYTON, PHILIP A	

ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
05/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No.	Applicant(s)	
	10/787,183	SAKAUE ET AL.	
	Examiner	Art Unit	
	Philip Guyton	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12,13,19 and 20* is/are rejected.

7)☒ Claim(s) *11,14-16 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 7-10, 13, 19 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,096,406 to Kanazawa et al. (hereinafter Kanazawa).

With respect to claim 1, Kanazawa discloses an ECC (Error check and Correct) control apparatus (figure 1, item 4) to be connected between a host (figure 1, item 1) and a memory (figure 1, item 3), comprising:

a data-path circuit (figure 1, items 5, 7) which inputs and outputs data to and from the host (column 5, lines 58-64), and inputs and outputs data to and from the memory (column 5, lines 48-57);

a detecting circuit which detects a protected-data region and a redundant region of write data input from the host and having a predetermined data length (column 5, lines 48-53 and column 10, lines 44-64);

a code-generating circuit which generates an error-correction code for correcting errors in data of the protected-data region (figure 18, item 20A and column 14, lines 43-51); and

a code-inserting circuit which inserts the error-correction code in the redundant region (figure 18, item 30 and column 14, line 61-column 15, line 13 and column 5, lines 51-53);

wherein the data-path circuit outputs the write data to the memory in synchronization with a first clock signal generated from a write-enable signal which is input from the host and indicates that data is being written into the memory (column 3, lines 34-35 and column 10, lines 65-67 and column 12, lines 44-49).

With respect to claim 2, Kanazawa discloses a counter which counts data items of the write data (column 3, lines 34-41), and in which the detecting circuit detects the protected-data region and redundant region of the write data in accordance with a count value obtained by the counter (column 10, line 65-column 11, line 3 and column 12, lines 44-49).

With respect to claim 3, Kanazawa discloses wherein the detecting circuit detects a specified part of the redundant region (figure 4, item 9 and column 8, lines 4-8), the code-generating circuit generates an error-correction code for correcting errors in the data of the protected-data region and the data of those parts of the redundant region which precede the specified part, and the code-inserting circuit inserts the error-correction code in the specified part of the redundant region (column 8, lines 33-40 and column 12, lines 20-27).

With respect to claim 4, Kanazawa discloses a syndrome circuit which performs an syndrome operation on a read data input from the memory and having the predetermined data length, by using the error-correction code contained in the read data, and which generates a syndrome signal, and an error-correcting circuit which corrects errors in accordance with the syndrome signal (column 13, lines 1-50).

With respect to claim 5, Kanazawa discloses wherein the error-correcting circuit comprises an error-presence/absence determining circuit which determines whether the read data contains errors, and an error-information generating circuit which generates correction information for correcting errors, when the error-presence/absence determining circuit determines that the read data contains errors (column 5, line 58-column 6, line 3 and column 8, lines 41-50).

With respect to claim 7, Kanazawa discloses wherein the error-information generating circuit generates normal-end information when the error-presence/absence determining circuit determines that the read data contains no errors (column 13, lines 19-22).

With respect to claim 8, Kanazawa discloses in which the counter counts pulses that constitute the write-enable signal, and which further comprises an enable interface circuit which does not output the write-enable signal to the memory when the number of pulses counted by the counter reaches a predetermined value (column 3, lines 34-41 and column 12, lines 44-49).

With respect to claim 9, Kanazawa discloses in which the counter counts pulses that constitute the read-enable signal, and which further comprises an enable interface

circuit which does not output the read-enable signal to the memory when the number of pulses counted by the counter reaches a predetermined value (column 3, lines 34-41 and column 12, lines 44-49).

With respect to claim 10, Kanazawa discloses wherein the counter starts counting the pulses after the data-path circuit receives an address signal that represents the address of the write data (column 7, lines 8-17).

With respect to claim 13, Kanazawa discloses a region-changing circuit which changes that part of the redundant region which is provided to store the error-correction code, and in which the code-inserting circuit inserts the error-correction code in that part of the redundant region which has been changed by the region-changing circuit (column 12, lines 20-27).

With respect to claim 19, Kanazawa discloses wherein the memory is a NAND flash memory (figure 2 and column 6, lines 4-6).

With respect to claim 20, Kanazawa discloses wherein the data-path circuit outputs the read data to the host in synchronization with a second clock signal generated from a read-enable signal which is input from the host and indicates that data is being read from memory (column 3, lines 35-37 and column 12, lines 44-49 and column 15, lines 1-6).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa in view of U.S. Patent No. 6,339,546 to Katayama et al. (hereinafter Katayama).

With respect to claim 6, Kanazawa does not disclose expressly wherein the error-presence/absence determining circuit determines whether the number of erroneous data items has exceeded a predetermined value, when the error-presence/absence determining circuit determines that the read data contains errors, and the error-information generating circuit generates abnormal-end information indicating that it is impossible to correct the read data, when the error-presence/absence determining circuit determines that the number of erroneous data items has exceeded the predetermined value.

Katayama teaches an ECC circuit that determines causes of errors in a flash memory device until a threshold number of errors are detected, whereupon it becomes impossible to continue using that storage element (column 2, lines 22-39).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Kanazawa by determining whether the number of erroneous data items has exceeded a predetermined value as taught by Katayama. A person of ordinary skill in the art would have been motivated to do so because Katayama teaches in which flash memory often becomes susceptible to errors based on normal use over a long period of time (column 1, line 27-column 2, line 19). Thus, the

technique of Katayama would have been highly desirable to Kanazawa in order to determine damaged memory locations, and thus avoid unnecessary errors.

With respect to claim 12, modified Kanazawa discloses in which the error-information generating circuit generates correction-end information when the error-presence/absence determining circuit determines that the number of erroneous data items has not exceeded the predetermined value (Katayama – column 4, line 62-column 5, line 12), and which further comprises an interruption circuit which generates and supplies an interruption signal to the host to interrupt the host and an information output circuit which outputs the normal-end information or the abnormal-end information to the host when the interruption circuit supplies the interruption signal to the host (column 13, lines 19-45).

Allowable Subject Matter

5. Claims 11, 14-16, and 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 6 March 2007 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies

(i.e., arrangement of ECC circuit so as to interrupt data bus) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant further argues Kanazawa does not teach or disclose generating a clock from an enable signal as recited in amended claim 1. The examiner respectfully disagrees. Kanazawa discloses an internal clock of the ECC control circuit that controls when write and read data is input or output between the memory and ECC circuits (column 3, lines 34-41). Additionally, the internal clock is provided in synchronization with the system clock (column 12, lines 44-49). Therefore, in this case, the system clock signal from the host is equivalent to a write-enable or read-enable signal, as it controls when writes and reads can occur.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Guyton whose telephone number is (571) 272-3807. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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5/2/07

ROBERT W. BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100